

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Hiatt et al.

Application No.: 10/733,226

Confirmation No.: 8010

Filed: December 10, 2003

Art Unit: 2811

For: MICROELECTRONIC DEVICES AND
METHODS FOR FILING VIAS IN
MICROELECTRONIC DEVICES

Examiner: C. A. Matthews

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This brief is filed in furtherance of the Notice of Appeal filed in this case on March 2, 2010.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1205.2:

- I. Real Party In Interest
- II Related Appeals and Interferences
- III. Status of Claims
- IV. Status of Amendments
- V. Summary of Claimed Subject Matter
- VI. Grounds of Rejection to be Reviewed on Appeal
- VII. Argument
- VIII. Claims Appendix
- IX. Evidence Appendix
- X. Related Proceedings Appendix

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

Micron Technology, Inc.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 23 claims pending in the application.

B. Current Status of Claims

1. Claims canceled: 1-27, 38 and 48
2. Claims withdrawn from consideration but not canceled: 37
3. Claims pending: 28-37, 39-47 and 49-52
4. Claims allowed: none
5. Claims rejected: 28-36, 39-47 and 49-52

C. Claims On Appeal

The claims on appeal are claims 28-36, 39-47 and 49-52.

IV. STATUS OF AMENDMENTS

Applicant did not file an Amendment After Final Rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

A. Background

Packaged microelectronic devices having microelectronic dies with integrated circuits are used in cell phones, pagers, personal digital assistants, computers, and many other electronic devices. Manufacturers are continuously trying to increase the performance of such devices, while reducing the size or “footprint” of the device on printed circuit boards. Reducing the size of the device can be difficult, however, because as the integrated circuitry becomes more sophisticated, it typically requires more bond-pads, which results in larger ball-grid arrays and thus larger footprints. (Specification at [0007]).

One technique for increasing the component density of microelectronic devices within a given footprint is to stack one device on top of the other in a wire-bonded, stacked-die arrangement. In this arrangement, each microelectronic device includes a die having an integrated circuit electrically coupled to a series of bond-pads. A redistribution layer electrically couples the bond-pads on each die to a plurality of corresponding solder balls. Wire-bonds extending from the solder balls on the first die to the solder balls on the second die electrically couple the first microelectronic device to the second microelectronic device. (Specification at [0008], Figure 1).

In the stacked-die arrangement described above, the solder balls on the second microelectronic device are positioned outside the perimeter of the first microelectronic device to facilitate installation of the wire-bonds extending between the corresponding solder balls. Positioning the solder balls on the second microelectronic device in this manner has the undesirable effect of increasing the footprint of the stacked-die arrangement. Moreover, installation of the wire-bonds can be a complex and/or expensive process because it requires placing the individual wires between pairs of closely-spaced solder balls. In addition, this type of installation may not be feasible for the high-density, fine-pitch ball grid arrays of some high-performance devices because the solder balls are spaced too close together to be connected to individual wire-bonds. (Specification at [0009], Figure 1).

B. Overview of Appellant's Technology

Appellant's technology is directed toward microelectronic devices, methods for packaging microelectronic devices, and methods for filling vias in dies and other substrates to form conductive interconnects. One method of forming a conductive interconnect in accordance with this technology includes, *inter alia*, providing at least one passage through a microfeature workpiece having a plurality of dies. The passage extends from a first side of the microfeature workpiece to a second side of the microfeature workpiece. The method can further include forming a conductive plug in the passage adjacent to the first side of the microelectronic workpiece. A conductive material can then be deposited in the passage to at least generally fill the passage from the conductive plug to the second side of the microelectronic workpiece. (Specification at [0019], Figure 3 and Figure 5A-8).

In a further embodiment of appellant's technology, a method of forming a conductive interconnect in a microelectronic device can include providing at least one passage through a microfeature workpiece having a plurality of dies. The passage can define a first opening in a first side of the microfeature workpiece and a second opening in a second side of the microfeature workpiece. The method can further include applying a sealing layer to the first side of the microfeature workpiece to at least generally seal the first opening of the passage. A first portion of conductive material can then be deposited through the second opening of the passage to form a plug in the passage adjacent to the sealing layer. After the plug has been formed, a second portion of conductive material can be deposited through the second opening of the passage to at least generally fill the passage from the plug to the second side of the microelectronic workpiece. (Specification at [0021], Figures 6A-6D).

C. Claim 28

Independent claim 28 is directed to a packaged microelectronic device comprising a die 212 having an integrated circuit 214 positioned between a first side 201 and an opposite second side 202. (E.g., Specification at [0025], Figure 2). The packaged microelectronic device further

comprises a bond-pad 216 positioned on the first side 201 of the die 212 and electrically coupled to the integrated circuit 214. (E.g., Specification at [0025] and [0031], Figures 2 and 5A). The packaged microelectronic device additionally comprises a passage 342, a first conductive material 560, and a second conductive material 545. (E.g., Specification at [0031], Figures 5A and 5B). The passage 342 extends completely through the die 212 and is aligned with and extends through the bond-pad 216. (E.g., Specification at [0027] and [0031], Figure 3). The first conductive material 560 is deposited in a first portion of the passage 342 adjacent to the first side 201 of the die 212 to form a conductive plug 560 electrically connected to the bond-pad 216. (E.g., Specification at [0031], Figure 5A). The second conductive material 545 is deposited in a second portion of the passage 342 in contact with the conductive plug 560 to at least generally fill the passage 342 from the conductive plug 560 to the second side 202 of the die 212. (E.g., Specification at [0031] and [0032], Figure 5B). The foregoing indications of reference numbers, Figures and Specification paragraphs are provided as examples of representative embodiments configured in accordance with independent claim 28.

D. Claim 33

Independent claim 33 is directed to a microfeature workpiece having a first side 201 and a second side 202. The microfeature workpiece comprises, *inter alia*, a passage 342 extending completely through a bond-pad 216 and a die 212 from the first side 201 of the microfeature workpiece to the second side 202 of the microfeature workpiece. (E.g., Specification at [0025] and [0031], Figures 2 and 5A). The microfeature workpiece further comprises a first conductive material 560 and a second conductive material 545. The first conductive material 560 is deposited in a first portion of the passage 342 adjacent to the first side 201 of the microfeature workpiece to form a conductive plug 560 in contact with the bond-pad 216. The second conductive material 545 is deposited in a second portion of the passage 342 in contact with the conductive plug 560 to at least generally fill the passage 342 from the conductive plug 560 to the second side 202 of the microfeature workpiece. (E.g., Specification at [0031] and [0032], Figures 5A and 5B). The first conductive material 560 is different than the second conductive material 545. (E.g., Specification at [0031] and [0032], Figure 5B). The foregoing indications

of reference numbers, Figures and Specification paragraphs are provided as examples of representative embodiments configured in accordance with independent claim 33.

E. Claim 39

Independent claim 39 is directed to a microelectronic device set comprising a first microelectronic device 210b having a first die 212 with a first bond-pad 216 electrically coupled to a first integrated circuit 214. (E.g., Specification at [0041], Figure 9). The first device 210b further includes a passage 342 extending completely through the first die 212 and the first bond-pad 216, and a conductive interconnect 546 deposited in the passage 342. The conductive interconnect 546 includes a first conductive material 560 deposited in a first portion of the passage 342 to form a conductive plug 560 having a boundary, and a second conductive material 545 deposited in a second portion of the passage 342 in contact with the boundary of the conductive plug 560 to at least generally fill the passage 342. (E.g., Specification at [0041], Figure 9). The microelectronic device set of claim 39 further includes at least a second microelectronic device 920 having a second die 912 with a second bond-pad 916 electrically coupled to a second integrated circuit 914. The second bond-pad 916 is electrically coupled to the conductive interconnect 546 of the first microelectronic device 210b. (E.g., Specification at [0041], Figure 9). The foregoing indications of reference numbers, Figures and Specification paragraphs are provided as examples of representative embodiments configured in accordance with independent claim 39.

F. Claim 44

Independent claim 44 is directed to a microelectronic device set comprising a first microelectronic device 210b and at least a second microelectronic device 920. The first microelectronic device includes a first die 212 and a conductive interconnect 546. The first die 212 includes a first bond-pad 216 electrically coupled to a first integrated circuit 214, and a passage 342 aligned with and extending through the first bond-pad 216. (E.g., Specification at [0041], Figure 9). The conductive interconnect 546 includes a first conductive material

deposited in a first portion of the passage 342 to form a conductive plug 560 in contact with the first bond-pad 216, and a second conductive material 545 deposited in a second portion of the passage 342 in contact with the conductive plug 560 to at least generally fill the passage. (E.g., Specification at [0041], Figure 9). The second microelectronic device has a second die 912 with a second bond-pad 916 electrically coupled to a second integrated circuit 914. The second bond-pad 916 is electrically coupled to the first bond-pad 216 of the first microelectronic device 210b. (E.g., Specification at [0041], Figure 9). The foregoing indications of reference numbers, Figures and Specification paragraphs are provided as examples of representative embodiments configured in accordance with independent claim 44.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(A) Whether claims 28 and 44 are unpatentable under 35 U.S.C. § 102(b) over U.S. Patent No. 6,459,150 to Wu et al. ("Wu");

(B) Whether claims 29, 30, 33, 36, 39-41, 43, 45 and 49-52 are unpatentable under 35 U.S.C. § 103(a) over the combination of Wu and U.S. Patent No. 6,809,421 to Hayasaka et al. ("Hayasaka");

(C) Whether claims 31, 34 and 46 are unpatentable under 35 U.S.C. § 103(a) over the combination of Wu and U.S. Patent Application Publication No. 2004/0023447 to Hirakata et al. ("Hirakata"), or the combination of Wu, Hayasaka, and Hirakata;

(D) Whether claims 32, 35 and 47 are unpatentable under 35 U.S.C. § 103(a) over the combination of Wu and U.S. Patent Application Publication No. 2004/0087441 to Bock et al. ("Bock"), or the combination of Wu, Hayasaka, and Bock; and

(E) Whether claim 42 is unpatentable under 35 U.S.C. § 103(a) over the combination of Wu, Hayasaka, and U.S. Patent No. 6,982,487 to Kim et al. ("Kim").

VII. ARGUMENT

A. The Patentability of the Claims1. Independent Claims 28 and 44

Independent claim 28 is directed to a packaged microelectronic device that includes, *inter alia*, a die having a bond-pad electrically coupled to an integrated circuit. A passage extends completely through the die and the bond-pad. A first conductive material is deposited in a first portion of the passage to form a conductive plug electrically connected to the bond-pad. A second conductive material is deposited in a second portion of the passage in contact with the conductive plug to at least generally fill the passage.

Independent claim 44 is directed to a microelectronic device set having a first microelectronic device and a second microelectronic device. The first microelectronic device includes, *inter alia*, a first die having a first bond-pad electrically coupled to a first integrated circuit. A passage extends through the first bond-pad. A conductive interconnect is deposited in the passage, and includes a first conductive material deposited in a first portion of the passage to form a conductive plug in contact with the bond-pad. The conductive interconnect further includes a second conductive material deposited in a second portion of the passage in contact with the conductive plug to at least generally fill the passage.

a. The Applied Reference (Wu)

Wu discloses a solder bump 90 connecting a conductive pad 82 on an electronic substrate 80 to a conductive pad 58 on a silicon wafer 50. (Wu, Figures 2E-2G, and column 8 at lines 39-51). The solder bump 90 is formed by flowing liquid solder material through an aperture 70 to fill a gap between the silicon wafer 50 and the substrate 80. (Wu, Figure 2F, and column 8 at lines 47-51). The solder bump 90 is then reflowed to form an integral solder ball 100 and conductive plug 92. (Wu, Figures 2F and 2G, and column 8 at lines 57-60). As Wu expressly

notes, the conductive plug 92 is "formed integrally" with the solder ball 100. (Wu in column 8 at lines 60-64).

b. Wu Fails to Teach Each and Every Element of Independent Claims 28 and 44

Independent claims 28 and 44 were rejected under 35 U.S.C. § 102(b) as being anticipated by Wu. To anticipate a claim, the reference must teach each and every element of the claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, the reference must show the identical invention in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). In the present case, however, Wu fails to teach each and every element of claims 28 and 44, much less show the identical invention in as complete detail as is contained in the claim.

For example, the packaged microelectronic device of claim 28 includes a *first* conductive material deposited in a first portion of the passage to form a conductive plug, and a *second* conductive material deposited in a second portion of the passage in contact with the conductive plug. Wu does not disclose or suggest first and second conductive materials. To the contrary, Wu repeatedly emphasizes that "the plurality of metal plugs 92 are formed integrally with the solder balls 100." (Wu in column 8, at lines 62-64).

The Examiner maintains that the solder bump 90 shown in Figure 2F of Wu constitutes the first conductive material of claim 28, and the metal plug 92 shown in Figure 2G of Wu constitutes the second conductive material of claim 28. This construction ignores the fact that the solder bump 90 and the metal plug 92 are integrally formed from the *same* conductive material during a single reflow process. (See, e.g., Wu in column 8 at lines 59-62: "*The solder bumps 90 are reflowed into solder balls 100...in the same reflow process, the solder material...forms a plurality of conductive plugs 92.*") Accordingly, the metal plug 92 of Wu is not a "second conductive material."

Although claim 28 specifically requires "a first conductive material deposited in a first portion of the passage; and a second conductive material deposited in a second portion of the passage," the Examiner continues to assert that "the claims do not require the first and second materials to be different nor do the claims preclude the first and second conductive materials from being formed integrally." (Office Action at 10). This assertion ignores some of the most basic tenets of US patent law. For example, it is well settled that "all words in a claim must be considered in judging the patentability of that claim against the prior art," and when considered, the words of the claim must be given their plain meaning unless the plain meaning is inconsistent with the specification. (*In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970); *In re Zletz*, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989)). In the present case, however, the Examiner has failed to consider or assign *any* meaning to the words "first" and "second" conductive material.

In addition, it is well settled law that the claims should be given their broadest *reasonable* construction "in light of the specification as it would be interpreted by one of ordinary skill in the art." *In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1364[, 70 USPQ2d 1827] (Fed. Cir. 2004). One of ordinary skill in the art interpreting the specification would clearly understand that the "first conductive material" forming the conductive plug is different than, or at least not formed integrally with, the "second conductive material" contacting the conductive plug. (See, for example, Figures 5A and 5B and the associated text at [0032]: "after the conductive plug 560 is in place, the remaining portion of the passage 342 can be filled with a conductive material 545" and "the conductive plug 560 can serve as an electrode for electroplating the passage 342 with a suitable material, such as copper.") In contrast to claims 28 and 44, Wu teaches an integrally formed conductive plug. Therefore, Wu cannot support a Section 102 rejection of independent claims 28 and 44, and the Board should reverse the rejection.

2. Dependent Claims 29, 45, 49 and 52

Claims 29, 45, 49 and 52 were rejected under 35 U.S.C. § 103(a) over the combination of Wu and Hayasaka. Claims 29 and 49 depend from base claim 28, and claims 45 and 52 depend

from base claim 44. Wu cannot support a Section 102 rejection of base claims 28 and 44 for at least the reasons discussed in detail above. Moreover, Hayasaka fails to cure the deficiencies of Wu with respect to base claims 28 and 44. Therefore, the proposed combination of Wu and Hayasaka cannot support a Section 103 rejection of dependent claims 29, 45, 49 and 52 for at least the reason that these references cannot support a Section 103 rejection of corresponding base claims 28 and 44, and for the additional features of these dependent claims. Therefore, the Board should reverse the rejection of dependent claims 29, 45, 49 and 52.

3. Dependent Claims 31, 32, 46 and 47

Claims 31 and 46 were rejected under 35 U.S.C. § 103(a) over the combination of Wu and Hirakata, or the combination of Wu, Hayasaka, and Hirakata. Claims 32 and 47 were rejected under 35 U.S.C. § 103(a) over the combination of Wu and Bock, or the combination of Wu, Hayasaka, and Bock.

Claims 31 and 32 depend from base claim 28, and claims 46 and 47 depend from base claim 44. Wu cannot support a Section 102 rejection of base claims 28 and 44 for at least the reasons discussed in detail above. Moreover, none of the additional references of Hirakata, Hayasaka, nor Bock, either alone or in combination, cure the deficiencies of Wu with respect to base claims 28 and 44. Accordingly, none of the proposed combinations of Wu, Hirakata, Bock, and/or Hayasaka can support a Section 103 rejection of dependent claims 31, 32, 46 and 47 for at least the reason that these references cannot support a Section 103 rejection of corresponding base claims 28 and 44, and for the additional features of these dependent claims. Therefore, the Board should reverse the rejection of dependent claims 31, 32, 46 and 47.

4. Independent Claim 33

Independent claim 33 is directed to a microfeature workpiece having a passage extending completely through a bond-pad and a die. A first conductive material is deposited in a first portion of the passage to form a conductive plug in contact with the bond-pad. A second conductive material is deposited in a second portion of the passage in contact with the

conductive plug. Claim 33 expressly states that the first conductive material is different than the second conductive material.

The Examiner acknowledges that Wu fails to teach the first and second conductive materials of claim 33. In an attempt to cure this deficiency, the Examiner makes the conclusory statement that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Wu to have the first conductive material different than the second conductive material as taught by Hayasaka." (Office Action at 5). Rejections based on obviousness, however, cannot be sustained with mere conclusory statements. (MPEP § 2142). At a minimum, the applied references must expressly or impliedly suggest the claimed invention or, if they do not, the Examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the references. (MPEP § 706.02(j)). In the present case, the applied references of Wu and Hayasaka do not suggest the claimed invention and the Examiner has not presented a convincing line of reasoning (or, indeed, *any* line of reasoning) as to why the artisan would have found the claimed invention to have been obvious in light of the references. Therefore, the Board should reverse the rejection of independent claim 33 for at least this reason.

Throughout Wu's disclosure, Wu emphasizes that the unique aspect of his single-step method is that "the bumping process and the bonding process are carried out simultaneously in a single step." (Wu in column 9 at lines 3-6, underlining added; and, e.g., Abstract; column 4 at lines 36 and 37; column 7 at lines 11 and 12; etc.). For example, Wu discloses that the solder material 90 fills up the aperture 70 and forms a plurality of conductive plugs 92 in a single reflow process. (Wu in column 8 at lines 60-62, Figures 2E-2G, underlining added). Accordingly, one of ordinary skill in the art would not have been motivated to modify the "single-step bumping/bonding method" taught by Wu to include two distinct steps of depositing two *different materials* in the passage, because doing so would destroy one of the express purposes of Wu's invention. Accordingly, the Board should reverse the rejection of independent claim 33 for this additional reason.

5. Independent Claim 39

It remains well settled law that the failure of an asserted combination to teach or suggest each and every feature of a claim is fatal to an obviousness rejection under 35 U.S.C. § 103. (*See In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)). In the present case, however, the proposed combination of Wu and Hayasaka fails to teach or suggest each and every feature of independent claim 39.

More specifically, claim 39 is directed to a microelectronic device set that includes, *inter alia*, a first die with a first bond-pad electrically coupled to a first integrated circuit, and at least a second die with a second bond-pad electrically coupled to a second integrated circuit. The Examiner maintains that Wu discloses such a microelectronic device set. More specifically, the Examiner identifies item 80 of Wu as “a first die (80).” (Office Action at page 5). Item 80 is not a die. In column 8 at lines 46-48, Wu expressly identifies item 80 as “i.e., a printed circuit board” formed “of an insulating material 88.” A printed circuit board formed of insulating material cannot reasonably be construed as “a first die with a first bond-pad electrically coupled to a first integrated circuit.” Accordingly, the Board should reverse the rejection of independent claim 39 for at least this reason.

The first microelectronic device of independent claim 39 includes a conductive interconnect formed from a first conductive material and a second conductive material. The first conductive material is deposited in a first portion of a passage to form a conductive plug, and the second conductive material is deposited in a second portion of the passage in contact with the conductive plug. More specifically, the first conductive material forms a boundary in the passage, and the second conductive material contacts the boundary.

The Examiner acknowledges that Wu fails to disclose a second conductive material in contact with a boundary of a conductive plug. (Office Action at page 6). In an attempt to cure this deficiency, the Examiner turns to Hayasaka and makes the unsupported assertion that it would have been obvious to modify Wu to use two different materials “in order to prevent device degradation [] due to diffusion of the conductive material (Hayasaka col. 14, lines 40-47).” The

Examiner's reliance on Hayasaka to provide the rationale for modifying Wu is misplaced and reflects a fundamental misunderstanding of Hayasaka.

More specifically, Hayasaka does not disclose or even suggest using two different materials to reduce device degradation. To the contrary, Hayasaka explicitly teaches forming the metal plug 15 (of, incidentally, a *single* material) after formation of the circuit devices to reduce device degradation. According to Hayasaka, the metal plug 15 should be formed after the circuit devices to reduce device degradation due to diffusion of the metal plug during the heat treatment necessary to form the circuit devices. (Hayasaka in column 14 at lines 32-42, Figure 7I). Accordingly, the Examiner has failed to provide a rationale basis as to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the references.

Moreover, the metal plug 15 of Hayasaka is formed from a single material, not two different materials. Although the solder bump 8 of Hayasaka *may* be formed from a different material than the metal plug 15 (*see*, e.g., Figure 17B of Hayasaka), this has nothing to do with device degradation and provides no motivation for modifying Wu in the proposed manner. Accordingly, the Board should reverse the rejection of independent claim 39.

6. Dependent Claims 30, 36, 50 and 51

Claims 30, 36, 50 and 51 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Wu and Hayasaka. Claims 36 and 50 depend from base claim 33, and claims 30 and 51 depend from base claim 39. The proposed combination of Wu and Hayasaka cannot support a Section 103 rejection of base claims 33 and 39 for at least the reasons discussed in detail above. Accordingly, the proposed combination of Wu and Hayasaka cannot support a Section 103 rejection of dependent claims 30, 36, 50 and 51 for at least the reason that these references cannot support a Section 103 rejection of corresponding base claims 33 and 39, and for the additional features of these dependent claims. Therefore, the Board should reverse the rejection of dependent claims 30, 36, 50 and 51.

7. Dependent Claims 34, 35 and 40-43

Claims 34, 35 and 40-43 were rejected under 35 U.S.C. § 103(a) as being unpatentable over various combinations of Wu and Hirakata, Bock, Hayasaka, and/or Kim. Claims 34 and 35 depend from base claim 33, and claims 40-43 depend from base claim 39. The combination of Wu and Hayasaka cannot support a Section 103 rejection of base claims 33 and 39 for at least the reasons discussed in detail above. Moreover, none of the applied references of Hirakata, Bock, or Kim cures the deficiencies of Wu and Hayasaka with respect to base claims 33 and 39. Accordingly, none of the proposed combinations of Wu and Hayasaka, Bock, Hirakata, and/or Kim can support a Section 103 rejection of dependent claims 34, 35 and 40-43 for at least the reason that none of these combinations can support a Section 103 rejection of corresponding base claims 33 or 39, and for the additional features of these dependent claims. Therefore, the Board should reverse the rejection of dependent claims 34, 35 and 40-43.

Please charge any underpayment of fees or credit any overpayment to our Deposit Account No. 50-0665, under Order No. 108298744US from which the undersigned is authorized to draw.

Dated:

June 2, 2010

Respectfully submitted,

By
Stephen E. Arnett

Registration No.: 47,392
PERKINS COIE LLP
P.O. Box 1247
Seattle, Washington 98111-1247
(206) 359-8000
(206) 359-7198 (Fax)
Attorney for Assignee

VIII. CLAIMS APPENDIX

28. A packaged microelectronic device comprising:
a die having a first side and a second side opposite to the first side, the die further having
an integrated circuit positioned between the first and second sides;
a bond-pad positioned on the first side of the die and electrically coupled to the integrated circuit;
a passage extending completely through the die and aligned with and extending through the bond-pad;
a first conductive material deposited in a first portion of the passage adjacent to the first side of the die to form a conductive plug electrically connected to the bond-pad;
and
a second conductive material deposited in a second portion of the passage in contact with the conductive plug to at least generally fill the passage from the conductive plug to the second side of the die.

29. The packaged microelectronic device of claim 28, further comprising an insulative layer deposited in the passage between the die and the first and second conductive materials.

30. The packaged microelectronic device of claim 29, further comprising an insulative layer deposited in the passage between the first die and the first and second conductive materials.

31. The packaged microelectronic device of claim 28 wherein the first conductive material includes an electronic ink in contact with an exposed surface of the bond-pad.

32. The packaged microelectronic device of claim 28 wherein the first conductive material includes a nano-particle deposition in contact with an exposed surface of the bond-pad.

33. A microfeature workpiece having a first side and a second side opposite to the first side, the microfeature workpiece comprising:

at least one die;

a bond-pad formed on the first side of the microfeature workpiece;

a passage extending completely through the bond-pad and the die from the first side of the microfeature workpiece to the second side of the microfeature workpiece;

a first conductive material deposited in a first portion of the passage adjacent to the first side of the microfeature workpiece to form a conductive plug in contact with the bond-pad; and

a second conductive material deposited in a second portion of the passage in contact with the conductive plug to at least generally fill the passage from the conductive plug to the second side of the microfeature workpiece, wherein the first conductive material is different than the second conductive material.

34. The microfeature workpiece of claim 33 wherein the first conductive material includes an electronic ink.

35. The microfeature workpiece of claim 33 wherein the first conductive material includes a nano-particle deposition.

36. The microfeature workpiece of claim 33, further comprising an insulative layer deposited in the passage between the die and the first and second conductive materials.

39. A microelectronic device set comprising:

a first microelectronic device having:

a first die with a first integrated circuit and a first bond-pad electrically coupled to the first integrated circuit, the first die further including a passage extending completely through the first die and the first bond-pad; and

a conductive interconnect deposited in the passage, the conductive interconnect including a first conductive material deposited in a first portion of the passage to form a conductive plug having a boundary in the passage, and a second conductive material deposited in a second portion of the passage in contact with the boundary of the conductive plug to at least generally fill the passage; and

at least a second microelectronic device having a second die with a second integrated circuit and a second bond-pad electrically coupled to the second integrated circuit, wherein the second bond-pad is electrically coupled to the conductive interconnect of the first microelectronic device.

40. The microelectronic device set of claim 39 wherein the first microelectronic device is attached to the second microelectronic device in a stacked-die arrangement.

41. The microelectronic device set of claim 39, further comprising a solder ball disposed between the conductive interconnect of the first microelectronic device and the second bond-pad of the second microelectronic device to electrically couple the first bond-pad to the second bond-pad.

42. The microelectronic device set of claim 39 wherein the passage is a first passage, wherein the second microelectronic device further includes a second passage extending through the second die and the second bond-pad, and wherein the second passage is completely filled with a third conductive material.

43. The microelectronic device set of claim 39 wherein the first microelectronic device further includes a redistribution layer formed on the first die, the redistribution layer including a conductive line having a first end portion attached to the first bond-pad and a second end portion positioned outward of the first end portion, wherein the second end portion is configured to receive electrical signals and transmit the signals to at least the first integrated circuit of the first die and the second integrated circuit of the second die.

44. A microelectronic device set comprising:

a first microelectronic device having:

a first die with a first integrated circuit and a first bond-pad electrically coupled to the first integrated circuit, the first die further including a passage aligned with and extending through the first bond-pad; and

a conductive interconnect deposited in the passage, the conductive interconnect including a first conductive material deposited in a first portion of the passage to form a conductive plug in contact with the bond-pad, and a second conductive material deposited in a second portion of the passage in contact with the conductive plug to at least generally fill the passage; and

at least a second microelectronic device having a second die with a second integrated circuit and a second bond-pad electrically coupled to the second integrated circuit, wherein the second bond-pad is electrically coupled to the first bond-pad of the first microelectronic device.

45. The packaged microelectronic device of claim 44, further comprising an insulative layer deposited in the passage between the first die and the first and second conductive materials.

46. The packaged microelectronic device of claim 44 wherein the first conductive material includes an electronic ink in contact with an exposed surface of the bond-pad.

47. The packaged microelectronic device of claim 44 wherein the first conductive material includes a nano-particle deposition in contact with an exposed surface of the bond-pad.

49. The packaged microelectronic device of claim 28, further comprising an insulative layer deposited in the passage, wherein the second conductive material contacts the conductive plug and the insulative layer.

50. The microfeature workpiece of claim 33, further comprising an insulative layer deposited in the passage, wherein the second conductive material contacts the conductive plug and the insulative material.

51. The microelectronic device set of claim 39 wherein the first microelectronic device further includes an insulative layer deposited in the passage, and wherein the second conductive material contacts the conductive plug and the insulative layer.

52. The microelectronic device set of claim 44 wherein the first microelectronic device further includes an insulative layer deposited in the passage, and wherein the second conductive material contacts the conductive plug and the insulative layer.

IX. EVIDENCE APPENDIX

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.

X. RELATED PROCEEDINGS APPENDIX

No related proceedings are referenced in Section II above, hence copies of decisions in related proceedings are not provided.